What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An interconnect structure for a semiconductor die, said interconnect structure comprising:

a conductive bond pad containing a copper layer; and

an implant region on at least an upper surface portion of said copper layer, said implant region containing titanium.

2. The interconnect structure of claim 1, wherein said implant region containing titanium has a thickness not greater than 1000Å.

3. The interconnect structure of claim 1, wherein said copper layer is elemental copper.

4. The interconnect structure of claim 1, wherein said copper layer contains a thin copper oxide layer thereon.

5. The interconnect structure of claim 4, wherein said copper oxide layer has a thickness not greater than 300Å.

6. The interconnect structure of claim 1, further comprising an electrical conductor bonded to said implant region containing titanium.

7. A chip interconnect bond comprising:

a conductive bond pad containing a copper layer;

an implant region on at least an upper surface portion of said copper layer, said implant region containing titanium; and

an electrically conductive bump bonded to said implant region containing titanium.

8. The interconnect bond of claim 7, wherein said implant region containing titanium has a thickness not greater than 1000Å.

9. The interconnect bond of claim 7, wherein said implant region containing titanium is approximately 50Å to 200Å thick.

10. The interconnect bond of claim 7, wherein said conductive bump is a solder ball.

11. The interconnect bond of claim 7, further comprising a circuit substrate bonded to said electrically conductive bump.

12. An integrated circuit comprising:

a semiconductor die having integrated circuitry formed on a substrate;

a conductive bond pad on a surface of said die and in electrical connection with said die integrated circuitry, said conductive bond pad having a copper layer;

an implant region on at least an upper surface portion of said copper layer, said implant region containing titanium;

an electrical conductor bonded to said implant region containing titanium; and

a circuit substrate having a bonding site, wherein said electrical conductor of said semiconductor die is bonded to said bonding site.

13. The integrated circuit of claim 12, wherein said implant region containing titanium is approximately 50Å to 200Å thick.

14. The integrated circuit of claim 12, wherein said electrical conductor is a wire bond.

15. The integrated circuit of claim 12, wherein said electrical conductor is a tape automated bond.

16. The integrated circuit of claim 12, wherein said electrical conductor is formed as a bump.

17. The integrated circuit of claim 12, wherein said electrical conductor is a conductive adhesive layer.

18. The integrated circuit of claim 12, wherein said electrical conductor is a solder ball.

19. An electronic circuit bonding interconnect structure, said structure comprising:

a bond pad having a copper layer, said copper layer being approximately 500Å to 20,000Å thick;

an implant region on at least an upper portion of said copper layer, said implant region containing titanium and being approximately 50Å to 200Å thick; and

an electrical conductor bonded to said titanium layer.

20. The electronic circuit bonding interconnect structure of claim 19, wherein said electrical conductor is a wire bond.

21. The electronic circuit bonding interconnect structure of claim 19, wherein said electrical conductor is a tape automated bond.

22. The electronic circuit bonding interconnect structure of claim 19, wherein said electrical conductor is a conductive adhesive layer.

23. The electronic circuit bonding interconnect structure of claim 19, wherein said electrical conductor is a solder ball.

24. A method of forming a copper-titanium interconnect, comprising the step of implanting at least one copper bond pad of a semiconductor die with titanium for a sufficient time to form an implanted titanium layer on said at least one bond pad.

25. The method of claim 24 further comprising the step of removing any copper oxide from said copper bond pad prior to said step of implanting said copper bond pad with titanium.

26. The method of claim 24, wherein said implanted titanium layer has a thickness within the range of approximately 50Å to 200Å.

27. The method of claim 24, wherein said at least one copper bond pad is implanted with Ti^+ at an energy level of 50keV and with a dosage of $5x10^{15}$ /cm^2.

28. A copper bond pad for a semiconductor device, said bond pad comprising:

a dielectric layer formed over a substrate of said semiconductor device;

a barrier layer formed over said dielectric layer;

a copper layer formed over said barrier layer, said copper layer having an upper surface implanted with titanium; and

an insulating layer over said copper layer having a via defining said bonding pad area.

29. The copper bond pad of claim 28, wherein said insulating layer further comprises an oxide layer over said insulating layer.

30. The copper bond pad of claim 28, wherein said dielectric layer is formed of a material selected from the group consisting of phosphosilicate glass, borophosphosilicate glass, silicon oxide, silicon nitride, and silicon oxynitride.

31. The copper bond pad of claim 28, wherein said barrier layer is formed of a material selected from the group consisting of silicon nitride,

titanium nitride, titanium tungsten, tantalum, tantalum nitride, a metal, a nitride, and a polycide.

32. The copper bond pad of claim 28, wherein said insulating layer is formed of a material selected from the group consisting of silicon nitride, silicon oxynitride, silicon oxide, phosphosilicate glass, borophosphosilicate glass, and a polyimide.

33. An interconnect structure for a semiconductor die, said interconnect structure comprising:

a conductive bond pad containing a copper layer; and

a titanium-aluminum barrier layer formed over at least an upper surface portion of said copper layer.

34. The interconnect structure of claim 33, wherein said copper layer is elemental copper.

35. The interconnect structure of claim 33, wherein said copper layer contains a thin copper oxide layer thereon.

36. The interconnect structure of claim 35, wherein said copper oxide layer has a thickness not greater than 300Å.

37. The interconnect structure of claim 33, wherein said upper surface portion of said copper layer is precleaned.

38. The interconnect structure of claim 33, wherein said titanium-aluminum barrier layer is annealed to form a titanium-aluminum-copper alloy.

39. The interconnect structure of claim 38, wherein said titanium-aluminum-copper alloy is annealed in the presence of nitrogen to form a titanium-aluminum-copper-nitrogen compound.

40. The interconnect structure of claim 33, further comprising an electrical conductor bonded to said titanium-aluminum barrier layer.

41. A method of forming a copper-titanium-aluminum interconnect comprising the step of forming a titanium-aluminum barrier layer over at least one copper bond pad of a semiconductor die.

42. The method of claim 41, wherein said titanium-aluminum barrier layer is deposited by sputtering.

43. The method of claim 42, wherein said deposited titanium-aluminum barrier layer is annealed to form a titanium-aluminum-copper alloy.

44. The method of claim 43, wherein said titanium-aluminum-copper alloy is annealed in the presence of nitrogen to form a titanium-aluminum- nitrogen compound.

45. The method of claim 41 further comprising removing any copper oxide from said copper bond pad prior to the formation of said titanium-aluminum barrier layer.

46. A chip interconnect bond comprising:

a conductive bond pad containing a copper layer;

a titanium-aluminum barrier layer formed over at least an upper surface portion of said copper layer; and

an electrically conductive bump bonded to said titanium-aluminum barrier layer.

47. The interconnect bond of claim 46, wherein said copper layer is elemental copper.

48. The interconnect bond of claim 46, wherein said copper layer contains a thin copper oxide layer thereon.

49. The interconnect bond of claim 48, wherein said copper oxide layer has a thickness not greater than 300Å.

50. The interconnect bond of claim 46, wherein said upper surface portion of said copper layer is precleaned.

51. The interconnect bond of claim 46, wherein said titanium-aluminum barrier layer is approximately 50Å to 200Å thick.

52. The interconnect bond of claim 46, wherein said titanium-aluminum barrier layer is annealed to form a titanium-aluminum-copper alloy.

53. The interconnect bond of claim 52, wherein said titanium-aluminum-copper alloy is annealed in the presence of nitrogen to form a titanium-aluminum-nitrogen compound.

54. The interconnect bond of claim 46, wherein said electrically conductive bump is a solder ball.

55. The interconnect bond of claim 46, further comprising a circuit substrate bonded to said electrically conductive bump.

56. A copper bond pad for a semiconductor device, said bond pad comprising:

a dielectric layer formed over a substrate of said semiconductor device;

a barrier layer formed over said dielectric layer;

a copper layer formed over said barrier layer, said copper layer having a titanium-aluminum layer formed over at least an upper surface portion of said copper layer; and

an insulating layer over said copper layer having a via defining said bond pad.

57. The copper bond pad of claim 56, wherein said insulating layer further comprises an oxide layer over said insulating layer.

58. The copper bond pad of claim 56, wherein said dielectric layer is formed of a material selected from the group consisting of phosphosilicate glass, borophosphosilicate glass, silicon oxide, silicon nitride, and silicon oxynitride.

59. The copper bond pad of claim 56, wherein said barrier layer is formed of a material selected from the group consisting of tantalum, tantalum nitride, tungsten, tungsten nitride, titanium nitride, titanium tungsten, a metal, a nitride, and a polycide.

60. The copper bond pad of claim 56, wherein said insulating layer is formed of a material selected from the group consisting of silicon nitride, silicon oxynitride, silicon oxide, phosphosilicate glass, borophosphosilicate glass, and a polyimide.

61. The copper bond pad of claim 56, wherein said titanium-aluminum layer is approximately 50Å to 200Å thick.

62. The copper bond pad of claim 56, wherein said titanium-aluminum barrier layer is annealed to form a titanium-aluminum-copper alloy.

63. The copper bond pad of claim 62, wherein said titanium-aluminum-copper alloy is annealed in the presence of nitrogen to form a titanium-aluminum-nitrogen compound.

64. The copper bond pad of claim 56, wherein said upper surface portion of said copper layer is precleaned.

65. An integrated circuit comprising:

a semiconductor die having integrated circuitry formed on a substrate;

a conductive bond pad on a surface of said die and in electrical connection with said die integrated circuitry, said conductive bond pad having a copper layer;

a titanium-aluminum layer formed over said copper layer;

an electrical conductor bonded to said titanium-aluminum layer; and

a circuit substrate having a bonding site, wherein said electrical conductor of said semiconductor die is bonded to said bonding site.

66. The integrated circuit of claim 65, wherein said titanium-aluminum layer is approximately 50Å to 200Å thick.

67. The integrated circuit of claim 65, wherein said electrical conductor is a wire bond.

68. The integrated circuit of claim 65, wherein said electrical conductor is a tape automated bond.

69. The integrated circuit of claim 65, wherein said electrical conductor is formed as a bump.

70. The integrated circuit of claim 65, wherein said electrical conductor is a conductive adhesive layer.

71. The integrated circuit of claim 65, wherein said electrical conductor is a solder ball.

72. The integrated circuit of claim 65, wherein said titanium-aluminum barrier layer is annealed to form a titanium-aluminum-copper alloy.

73. The copper bond pad of claim 72, wherein said titanium-aluminum-copper alloy is annealed in the presence of nitrogen to form a titanium-aluminum-nitrogen compound.